

1 Amendments to the Claims:

2 This listing of claims will replace all prior versions, and
3 listings, of claims in the application using (Original) (Currently
4 Amended) (New) (Canceled) (Previously Presented) nomenclature, as
5 recited in the below listing of claims.

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8 1. (Original) A system for channelizing an IF wideband input signal
9 into separated channelized digital output signals, the system
10 comprising,

11 a complex mixer for quadrature demodulation of the IF wideband
12 input signal into a complex signal,

13 a polyphase clock generator for generating polyphase clock
14 signals each having the same clocking signal that is staggered in
15 phase over a clock cycle,

16 a parallel converter comprising a bank of samplers for
17 respective sampling the complex signal into staggered sampled
18 complex signals and comprising a bank of converters for converting
19 the staggered sampled complex signals into respective sampled
20 digital complex signals, each of the samplers of the bank of
21 samplers sampling the complex signals at a rate of the clock cycle
22 at a respective staggered phase, and

23 a parallel filter bank comprising a polyphase filter bank of
24 filters for respective filtering the sampled digital complex
25 signals into respective filtered complex signals and comprising a
26 processor for transforming the filtered complex signals into the
27 channelized digital output signals.

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1 2. (Currently Amended) A system for channelizing an IF wideband
2 input signal into separated channelized digital output signals, the
3 system comprising,

4 a complex mixer for quadrature demodulation of the IF wideband
5 input signal into a complex signal,

6 a polyphase clock generator for generating polyphase clock
7 signals each having the same clocking signal that is staggered in
8 phase over a clock cycle,

9 a parallel converter comprising a bank of samplers for
10 respective sampling the complex signal into staggered sampled
11 complex signals and comprising a bank of converters for converting
12 the staggered sampled complex signals into respective sampled
13 digital complex signals, each of the samplers of the bank of
14 samplers sampling the complex signals at a rate of the clock cycle
15 at a respective staggered phase, and

16 a parallel filter bank comprising a polyphase filter bank of
17 filters for respective filtering the sampled digital complex
18 signals into respective filtered complex signals and comprising a
19 processor for transforming the filtered complex signals into the
20 channelized digital output signals, The system of claim 1 wherein,

21 the processor is a Fast Fourier Transform processor for computing
22 N point Fast Fourier transforms of the N filter complex signals
23 once every clock cycle of $(f_g/N)^{-1}$ seconds.

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26 3. (Currently Amended) The system of claim 1 2 wherein,

27 the polyphase filter bank comprises a plurality of digital
28 filters each of which is a finite impulse response filter.

1 4. (Currently Amended) The system of claim 1 2 wherein,

2 the polyphase filter bank comprises a plurality of digital
3 filters each of which is an infinite impulse response filter.

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5 5. (Currently Amended) The system of claim 1 2 wherein,

6 the input signal comprises a plurality of channel signals that
7 are frequency division multiple access signals having a channel
8 bandwidth, and

9 the polyphase filter bank comprises a plurality of digital
10 filters each of which having a bandwidth equal to 1/2 of a
11 bandwidth of a respective channel signal in the input signal.

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14 6. (Currently Amended) The system of claim 1 2 wherein,

15 the input signal is an IF wideband signal communicating channel
16 signals communicated within a channel bandwidth,

17 the complex signal comprises I and Q quadrature baseband
18 signals,

19 the staggered sampled complex signals are staggered sampled I
20 and Q quadrature baseband signals,

21 the sampled digital complex signals are digitized staggered
22 sampled I and Q quadrature baseband signals,

23 the filtered complex signals are baseband channel signals
24 within 1/2 of the channel bandwidth, and

25 the channelized digital output signals are separated baseband
26 channel signals.

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1 7. (Original) A system for channelizing an IF wideband signal into
2 channelized digital output signals, the system comprising,
3 a complex mixer for quadrature demodulation of the IF wideband
4 signal into a complex signal communicating channel signals
5 communicated within a channel bandwidth, the complex signal
6 comprises I and Q quadrature baseband signals,
7 a polyphase clock generator for generating polyphase clock
8 signals each of which having the same clocking signal that is
9 staggered in phase over a clock cycle,
10 a bank of samplers for respective sampling the I and Q baseband
11 quadrature signals into staggered sampled I and Q quadrature
12 signals, each of the samplers of the bank of sampler sampling the I
13 and Q quadrature signals at a rate of the clock cycle at a
14 respective staggered phase,
15 a bank of converters for converting the staggered sampled I and
16 Q quadrature signals into respective sampled digital I and Q
17 quadrature signals,
18 a polyphase filter bank of filters for respective filtering
19 the sampled digital I and Q quadrature signals into respective
20 filtered I and Q quadrature signals, and
21 a processor for transforming the filtered I and Q quadrature
22 signals into the channelized digital output signals.

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1 8. (Original) The system of claim 7 wherein,

2 the processor is a Fast Fourier Transform processor for
3 computing N point Fast Fourier transforms of the N filter complex
4 signals once every clock cycle of $(f_s/N)^{-1}$ seconds, and

5 the polyphase filter bank comprises a plurality of digital
6 filters each of which is a finite impulse response filter.

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8 9. (Original) The system of claim 7 wherein,

9 the IF wideband signal comprises a plurality of channel
10 signals that are in frequency division multiple access signals
11 having a channel bandwidth, and

12 the polyphase filter bank comprises a plurality of digital
13 filters each of which having a bandwidth equal to 1/2 of a
14 bandwidth of a respective channel signal in the input signal.

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